

In the Specification:

Replace the paragraph bridging pages 5 and 6 with the paragraph below.

A1

The Programmable Logic Core (PLC) is a very high density, high-speed configurable logic structure for use in the development of ASIC components. As illustrated in FIG. 2, the PLC is based on an array of Configurable Arithmetic Logic Units (CALUs) called the Multi-Scale Array (MSA). This structure directly supports functions of different scales, such as Register Transfer Level (RTL) functions (e.g., counters and adders) as well as complex state machine and random logic structures. Scratchpad memory blocks may be incorporated into a specific PLC Core to supplement the internal register storage capabilities of the MSA for datapath intensive applications. The Application Circuit Interface (ACI) provides the signal interface between the MSA programmable routing resources and the application circuitry. The ACI is optimized for each PLC Core and includes scan test registers which allow effective testing of the PLC independent of the application specific circuits, testing of the application specific circuits independent of the PLC and concurrent testing of the combined PLC and application specific circuit behavior. The PLC Control block provides control mechanisms for loading configuration data into the MSA, controlling the application clock and reset signals and for testing the PLC blocks.

Replace the full paragraph in the middle of page 6 with the paragraph below.

A2

The MSA can be implemented, for example, by the techniques disclosed in co-pending U.S. Appln. No. 09/475,400, commonly owned by the assignee of the present invention, the contents of which are incorporated fully herein by reference. Although an MSA based on the principles of the co-pending application is considered preferable, the present invention is not limited thereto, and those skilled in the art will be able to understand how to extend the principles of the invention to other types of programmable logic structures after being taught by the present disclosure.